

VHDL Code for CPLD game

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity game is
    port(switch : in STD_LOGIC;
         clk : in STD_LOGIC;
         pwin : out STD_LOGIC;
         plose : out STD_LOGIC;
         over : out STD_LOGIC;
         press : out STD_LOGIC;
         display1 : out STD_LOGIC_VECTOR(6 downto 0);
         display2 : out STD_LOGIC_VECTOR(6 downto 0)
    );
end game;

architecture behav of game is
    signal eq53,eq42,eq61,enb,match,latch_old,d_enb : STD_LOGIC;
    shared variable counter1 : integer range 0 to 7;
    shared variable counter2 : integer range 0 to 7;
    signal sum: integer range 0 to 12;
    signal reg : integer range 0 to 12;
    signal output : STD_LOGIC_VECTOR(6 downto 0);
    type STATE_TYPE is (reset,enb_c,win,lose,nop1,latch,nop2,stage2,enb_c1);
begin

    controlPath : process (clk,eq53,eq42,match)
        variable state : STATE_TYPE;
        begin

            if (clk'event and clk = '1') then

                CASE state is

                    WHEN reset => output<= "0011010";
                        if(switch = '0') then
                            state:=enb_c;
                        end if;

                    WHEN enb_c => output<= "1011110";
```

```

        if(switch = '1') then
            state:=nop1;
            output(6)<='0';
        end if;

    WHEN nop1 => output<="0011111";
        if eq53 = '1' then
            state:=win;
        elsif eq42 = '1' then
            state:=lose;
        else
            state:=latch;
        end if;

    WHEN win => output<="0001001";
        if switch='0' then
            state:=enb_c;
        end if;

    WHEN lose =>output<="0010001";
        if switch='0' then
            state:=enb_c;
        end if;

    WHEN latch =>output<="0111111";
        state:=stage2;

    WHEN nop2 => output<="0011111";
        if match = '1' then
            state:=win;
        else
            state:=lose;
        end if;

    WHEN enb_c1 =>output<="1011110";
        if(switch = '1') then
            state:=nop2;
            output(6)<='0';
        end if;

    WHEN stage2 =>output<="0011011";
        if(switch = '0') then
            state:=enb_c1;
        end if;

END CASE;

```

```
end if;
```

```
end process controlPath;
```

```
DATAFLOW : BLOCK
```

```
BEGIN
```

```
counter :process(clk)
```

```
begin
```

```
if(clk'event and clk = '1' and enb = '1') then
```

```
counter1 := counter1+1;
```

```
if(counter1 > 6) then
```

```
counter1 := 1;
```

```
counter2:=counter2+1;
```

```
if(counter2>6) then
```

```
counter2:=1;
```

```
end if;
```

```
end if;
```

```
sum <= counter1 + counter2;
```

```
end if;
```

```
end process counter;
```

```
eq53 <= '1' WHEN sum = 5 ELSE
```

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'1' WHEN sum = 3 ELSE
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```
'1' WHEN sum = 7 ELSE
```

```
'0';
```

```
eq42 <= '1' WHEN sum = 2 ELSE
```

```
'1' WHEN sum = 4 ELSE
```

```
'1' WHEN sum = 6 ELSE
```

```
'0';
```

```
reg_latch: process(latch_old)
```

```
begin
```

```
if(latch_old'event and latch_old = '1') then
```

```
reg<=sum;
```

```
end if;
```

```
end process reg_latch;
```

```
match <= '1' WHEN reg = sum ELSE '0';
```

```

display1 <= "1111111" WHEN d_enb = '0' ELSE
    "1001111" WHEN counter1 = 1 ELSE
        "0010010" WHEN counter1 = 2 ELSE
            "0000110" WHEN counter1 = 3 ELSE
                "1001100" WHEN counter1 = 4 ELSE
                    "0100100" WHEN counter1 = 5 ELSE
                        "0100000" when counter1 = 6 ELSE
                            "0001111" when counter1 = 7 else
                                "0000000" when counter1 = 8 else
                                    "0001100" when counter1 = 9;
display2 <= "1111111" WHEN d_enb = '0' ELSE
    "1001111" WHEN counter2 = 1 ELSE
        "0010010" WHEN counter2 = 2 ELSE
            "0000110" WHEN counter2 = 3 ELSE
                "1001100" WHEN counter2 = 4 ELSE
                    "0100100" WHEN counter2 = 5 ELSE
                        "0100000";
pwin <=output(4);
plose <=output(3);
press <= output(2);
over<= output(1);
enb<=output(6);
latch_old<=output(5);
d_enb<=output(0);

```

```

END BLOCK DATAFLOW;

```

```

end behav;

```